**Question 1 Report**

There are no significant special code implementations or usage instructions. The Verilog Modules for Parts A-E are all implemented as separate modules in ***Question1.v.*** The Testbench instantiates all 5 different modules in the same TB under the same test conditions using outputs ***outA-outE***, to compare the results of each implementation. However, the different modules seemed to be implemented differently in RTL, as shown below:

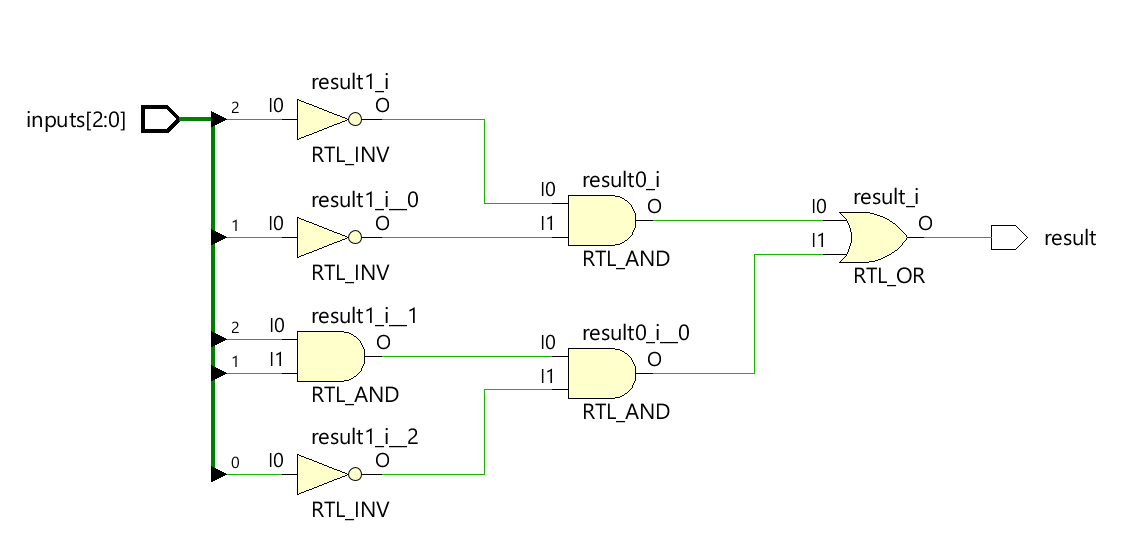


Figure - Concurrent Assignment

This is implemented directly using RTL Logic. The reduced equation for this circuit is ~A~B + AB~C, and as shown this is implemented using Inverters and 2 input AND/OR Gates.

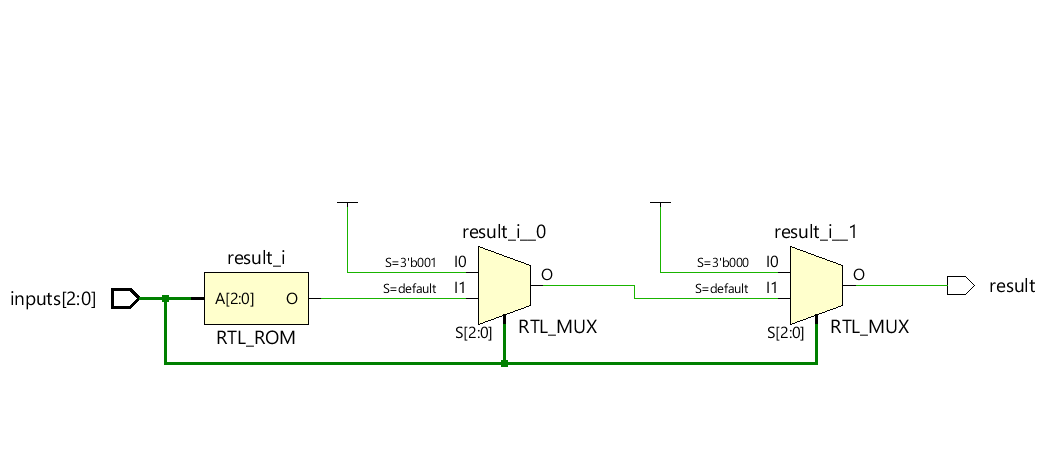


Figure - IF implementation

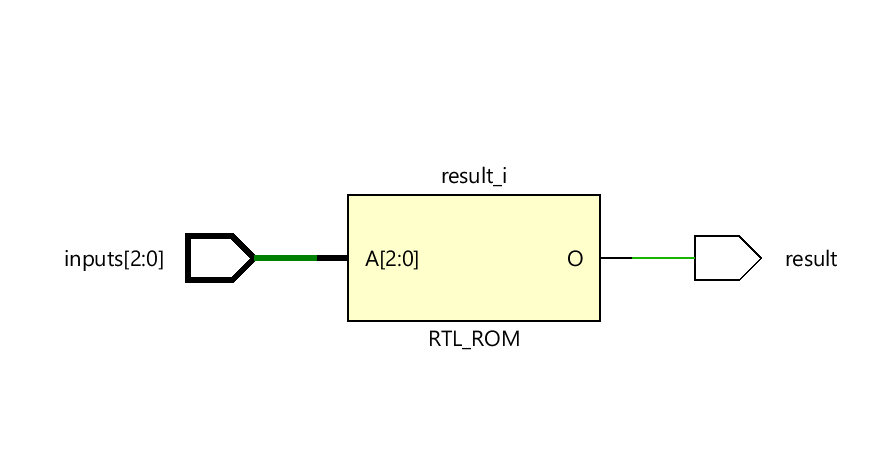


Figure - CASE Implementation

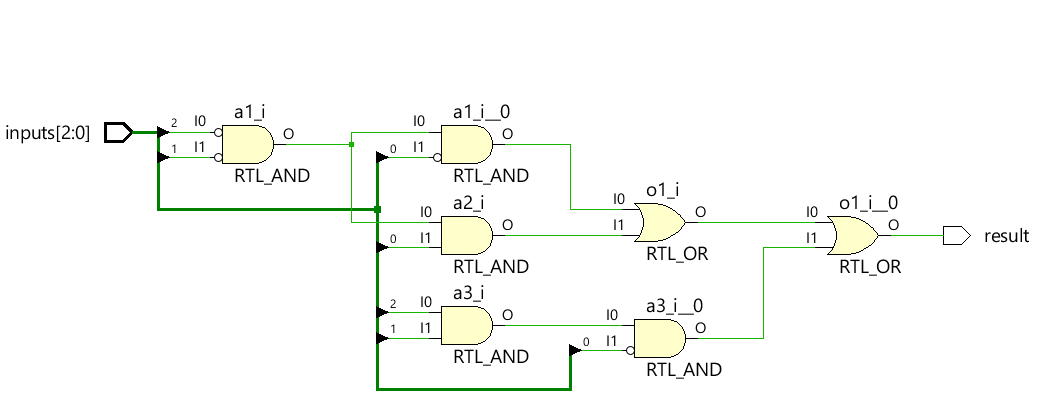


Figure - Structural Implementation

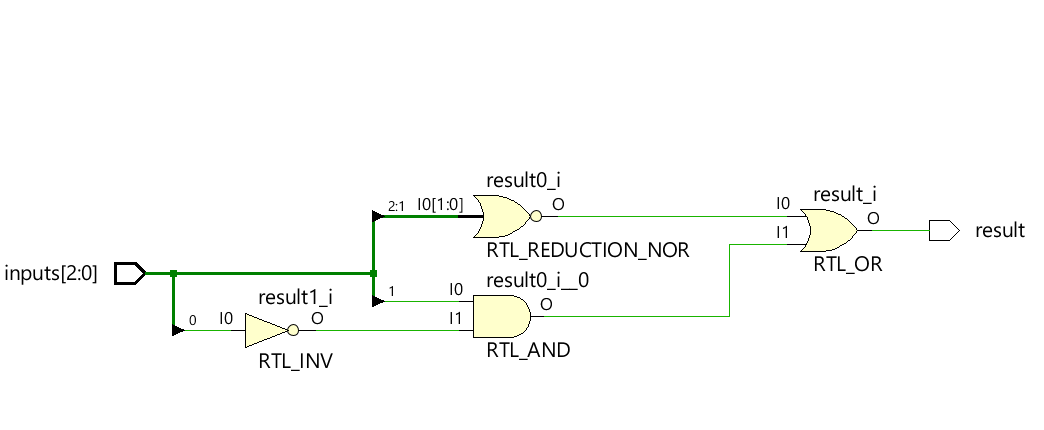


Figure - Reduction Operators

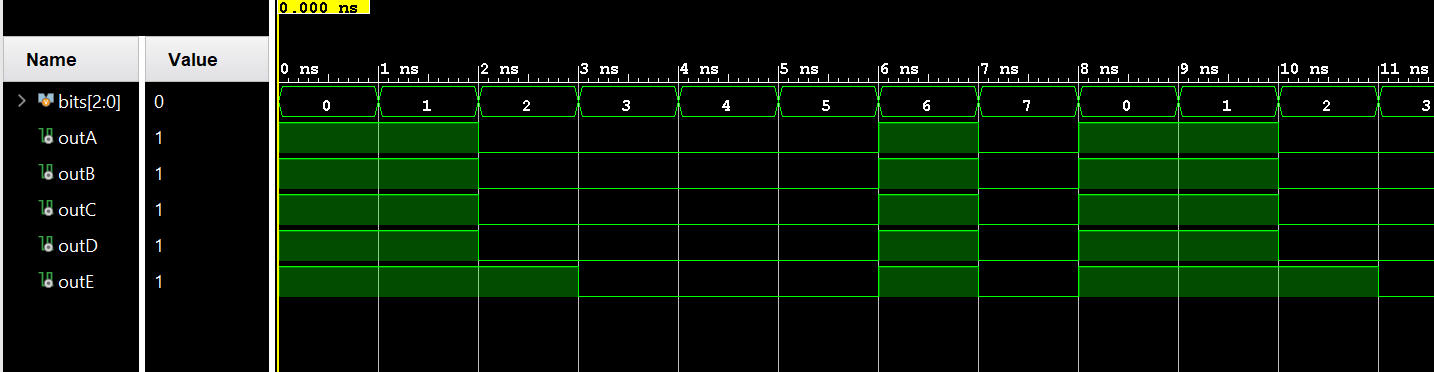


Figure – Outputs

As shown, all outputs have identical results except for 2, which is ~AB~C, a don’t care condition as shown in the assignment. OutA – OutE are the outputs for parts A-E.